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10/733,377	12/12/2003	Kazuhito Ichinose	501.43296X00	8552

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/733,377	ICHINOSE ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/733,377. Currently, claims 1-19 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. *Claims 1and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue (6,136,699).*

The Inoue patent (Inoue) discloses a fabrication method of a semiconductor integrated circuit device (figs. 6A-6D and col. 10, line 9 – col. 11, line 34). The method comprises: a first step of depositing a cobalt film 32 over the main surface of a silicon substrate 21, as recited in claim 1 (fig. 6B and col. 10, lines 56-58); and a second step of heat treating the substrate to form a silicide layer on the interface between the substrate and the cobalt film, as recited in claim 1 (col. 10, line 60 – col. 11, line 28). The cobalt film is deposited at a temperature lower than a temperature at which a reaction layer

of silicon and cobalt is formed on the interface between the silicon substrate and the cobalt film.[1]

The heat treatment of the substrate comprises: (a) first-stage heat treatment for forming a silicide layer having, as a main component, dicobalt silicide (Co_2Si) on the interface between the substrate and the cobalt film, as recited in claim 5 (col. 10, line 64 – col. 11, line 4); second-stage heat treatment for converting the main component of the silicide layer from dicobalt silicide into cobalt monosilicide (CoSi), as recited in claim 5 (col. 11, lines 15-20); and third-stage heat treatment for converting the main component of the silicide layer from cobalt monosilicide to cobalt to disilicide ($CoSi_2$), as recited in claim 5 (col. 11, lines 23-28). An unreacted portion of the cobalt film is removed from the main surface of the substrate (col. 11, lines 5-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

[1] A reaction between the substrate and the cobalt film does not occur until the first-stage heat treatment is performed (col. 10, line 64 – col. 11, line 4). Hence, the deposition temperature of the cobalt film, 450°C, is lower than a temperature at which a reaction layer of silicon and cobalt is formed.

3. *Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US 6,136,699) in view of Murphy et al. (US 6,117,771).*

As previously stated, Inoue discloses a second step of performing a heat treatment to form a silicide layer on the interface between the substrate and the cobalt film. While Inoue discloses a heat treatment, Inoue lacks anticipation of depositing the cobalt film at a temperature less than 200°C, as recited in claim 2; at a temperature less than 100°C, as recited in claim 3; and at a temperature less than 50°C, as recited in claim 4.

The Murphy et al. patent (Murphy) discloses a method for depositing a cobalt film on a silicon substrate (col. 2, lines 45-52 and col. 4, lines 31-55). The method comprises: a first step of depositing a cobalt film over the main surface of the substrate (col. 4, lines 31-43); and a second step of heat treating the substrate to form a silicide layer on an interface between the substrate and the cobalt film (col. 4, lines 44-55), wherein the cobalt film is deposited at a temperature within the low temperature range of about 20°C to 300°C (col. 1, lines 41-43).

Both Inoue and Murphy are from the same field of endeavor, methods of manufacturing semiconductor devices. Hence, the teaching for which Murphy is relied upon would have been recognized in Inoue by one of ordinary skill in the art at the time the invention was made.

The semiconductor device in Inoue comprises source/drain regions 29 and 30, which are formed prior to the deposition of cobalt film 32 (Inoue - fig. 6B and col. 9, lines 40-47 and 56-59). Diffusion of dopant impurities in the source/drain regions occurs during subsequent high temperature processes. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Inoue in view of Murphy by depositing the cobalt film at low temperatures, as taught by Murphy, because the low temperature deposition process helps to reduce diffusion of dopant impurities in the source/drain regions.

4. *Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US 6,136,699) in view of Agnello et al. (6,440,851 B1).*

The temperature of the third-stage heat treatment falls within a range of 700°C or greater but less than 900°C (col. 11, lines 23-28). While Inoue discloses a third-stage heat treatment within the range of 700°C to 900°C, Inoue lacks anticipation of: performing the first-stage heat treatment at a temperature that falls within a range of 200°C or greater but less than 400°C, as recited in claim 6; and performing the second-stage heat treatment at a temperature that falls within a range of 400°C or greater but less than 700°C, as recited in claim 6. In addition, Inoue lacks anticipation of depositing an

oxidation barrier film over the cobalt film, between the first and second steps, as recited in claim 7.

The Agnello et al. patent (Agnello) discloses a method for forming a cobalt disilicide film (figs. 1a-1f and col. 4, line 2 – col. 6, line 17). The method comprises a first step of depositing a cobalt alloy film 14 on a silicon substrate 10 (fig. 1a; col. 4, lines 2-4; and col. 4, lines 32-35), and a second step of heat-treating the substrate to form a cobalt disilicide layer (col. 5, line 13 – col. 6, line 11). The heat treatment comprises a first-stage heat treatment (col. 5, lines 13-26), a second-stage heat treatment (col. 5, lines 26-43), and a third-stage heat treatment (col. 5, line 66 – col. 6, line 11). The first-stage heat treatment falls within a range of 200°C or greater but less than 400°C (col. 5, lines 16-23). The second-stage heat treatment falls within a range of 400°C or greater but less than 700°C (col. 5, lines 26-37). The first-stage heat treatment forms a dicobalt silicide film (M_2XSi) (col. 5, lines 13-17). The second-stage heat treatment forms a cobalt monosilicide film (MXSi) (col. 5, lines 26-31).

Agnello further teaches depositing an oxidation barrier film over the cobalt alloy film, between the first and second steps (fig. 1b and col. 4, lines 57-58). The oxidation barrier layer prevents the diffusion of oxygen and other ambient gases into the structure (col. 4, line 66 – col. 5, line 3).

Both Inoue and Agnello are from the same field of endeavor, methods of manufacturing semiconductor devices. Hence, the teaching for which Agnello

is relied upon would have been recognized in Inoue by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Inoue in view of Agnello by performing the first and second-stage heat treatments at temperatures within the claimed temperature ranges, as taught by Agnello, because performing the first and second-stage heat treatments at such temperatures is sufficient to form a dicobalt silicide film and a cobalt monosilicide film, respectively. Furthermore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Inoue in view of Agnello by depositing an oxidation barrier film over the cobalt film, as taught by Agnello, because the oxidation barrier film prevents the diffusion of oxygen and other ambient gases from diffusing into the structure.

5. *Claims 8 and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue in view of Agnello et al.*

As previously stated, Inoue discloses a fabrication method of a semiconductor integrated circuit device (figs. 6A-6D and col. 10, line 9 – col. 11, line 34). The method comprises the steps of: forming a MISFET having a source and a drain 29 and 30 made of a pair of semiconductor regions formed over the main surface of a silicon substrate 21, as recited in claim 17 (fig. 6B and col. 10, lines 40-47), a gate insulating film 24 formed over the main surface of the substrate, as recited in claim 17 (fig. 6A and col. 10, lines 22-

26), and a gate electrode 25 formed over the gate insulating film, as recited in claim 17 (fig. 6A and col. 10, lines 25-32); depositing a cobalt film 32 over the main surface of a silicon wafer 21, as recited in claims 8 and 17, wherein the cobalt film is deposited in a first sputtering chamber of a sputtering apparatus equipped with a plurality of chambers including at least a sputtering chamber and a heat treatment chamber, as recited in claim 8 (fig. 6B and col. 10, lines 56-64); forming, in a second sputtering chamber, a silicide layer having dicobalt silicide (Co_2Si) as a main component over the interface between the silicon wafer and the cobalt film by a first-stage heat treatment, as recited in claims 8 and 17 (col. 10, line 64 – col. 11, line 4); converting the main component of the silicide layer from dicobalt silicide to cobalt monosilicide (CoSi) by a second-stage heat treatment in which the silicon wafer is heated to a temperature higher than the temperature of the first-stage heat treatment, as recited in claims 8 and 17 (col. 11, lines 15-20); and converting the main component of the silicide layer from the cobalt monosilicide to cobalt disilicide ($CoSi_2$) by a third-stage heat treatment in which the silicon wafer is heated at a temperature higher than the temperature of the second-stage heat treatment, as recited in claims 8 and 17 (col. 11, lines 23-28). The temperature of the third-stage heat treatment falls within a range of 700°C or greater but less than 900°C, as recited in claims 15 and 19 (col. 11, lines 23-28).

Inoue lacks anticipation of: depositing an oxidation barrier film over the main surface of the silicon wafer having the cobalt film deposited there over, as

recited in claims 8 and 17; removing the oxidation barrier film and an unreacted portion of the cobalt film from the main surface of the silicon wafer after the second-stage heat treatment, as recited in claims 8 and 17; performing the first-stage heat treatment at a temperature that falls within a range of 200°C or greater but less than 400°C, as recited in claims 13; and performing the second-stage heat treatment at a temperature that falls within a range of 400°C or greater but less than 700°C, as recited in claims 14.

Agnello discloses a method for forming a cobalt disilicide film (figs. 1a-1f and col. 4, line 2 – col. 6, line 17). The method comprises a first step of depositing a cobalt alloy film 14 on a silicon wafer 10 (fig. 1a; col. 4, lines 2-4; and col. 4, lines 32-35), and a second step of heat-treating the wafer to form a cobalt disilicide layer (col. 5, line 13 – col. 6, line 11). The heat treatment comprises a first-stage heat treatment (col. 5, lines 13-26), a second-stage heat treatment (col. 5, lines 26-43), and a third-stage heat treatment (col. 5, line 66 – col. 6, line 11). The first-stage heat treatment falls within a range of 200°C or greater but less than 400°C (col. 5, lines 16-23). The second-stage heat treatment falls within a range of 400°C or greater but less than 700°C (col. 5, lines 26-37).

Agnello further teaches depositing an oxidation barrier film over the cobalt alloy film (fig. 1b and col. 4, lines 57-58), and removing the oxidation barrier layer and an unreacted portion of the cobalt alloy film from the main

surface of the silicon wafer after the second-stage heat treatment (col. 5, lines 43-48).

Both Inoue and Agnello are from the same field of endeavor, methods of manufacturing semiconductor devices. Hence, the teaching for which Agnello is relied upon would have been recognized in Inoue by one of ordinary skill in the art at the time the invention was made.

Again, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Inoue in view of Agnello by performing the first and second-stage heat treatments at temperatures within the claimed temperature ranges, as taught by Agnello, because performing the first and second-stage heat treatments at such temperatures is sufficient to form a dicobalt silicide film and a cobalt monosilicide film, respectively. Again, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Inoue in view of Agnello by depositing an oxidation barrier film over the cobalt film, as taught by Agnello, because the oxidation barrier film prevents the diffusion of oxygen and other ambient gases from diffusing into the structure.

In Inoue, the unreacted portions of the cobalt film are removed after the first-stage heat treatment (col. 11, lines 5-15). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Inoue in view of Agnello by removing the oxidation barrier layer and unreacted portions of the cobalt film from a main surface of the wafer after the second-

stage heat treatment and not the first-stage heat treatment, as taught by Agnello, because it has been held that selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results (See *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946)).

Inoue does not teach that the temperature of the first-stage heat treatment is equal to the deposition temperature of the oxidation barrier film. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to perform the first-stage heat treatment at the same temperature as that of the deposition temperature of the oxidation barrier film, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art (See *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980)).

Inoue does not teach that the deposition time of the cobalt film and the deposition time of the oxidation barrier film in the step are each less than 15 seconds. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to deposit both the cobalt film and the oxidation barrier film at a deposition time less than 15 seconds, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves routine skill in the art (See *In re Aller*, 105 USPQ 233).

6. *Claims 9-11, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue in view of Agnello et al. as applied respectively to claims 8 and 17 above, and further in view of Murphy.*

Inoue lacks anticipation of: depositing the cobalt film at a temperature less than 200°C, as recited in claims 9 and 18; at a temperature less than 100°C, as recited in claims 10 and 18; and at a temperature less than 50°C, as recited in claims 11 and 18.

As previously stated, Murphy discloses a method for depositing a cobalt film on a silicon substrate (col. 2, lines 45-52 and col. 4, lines 31-55). The method comprises: a first step of depositing a cobalt film over the main surface of the substrate (col. 4, lines 31-43); and a second step of heat treating the substrate to form a silicide layer on an interface between the substrate and the cobalt film (col. 4, lines 44-55), wherein the cobalt film is deposited at a temperature within the low temperature range of about 20°C to 300°C (col. 1, lines 41-43).

Both Inoue and Murphy are from the same field of endeavor, methods of manufacturing semiconductor devices. Hence, the teaching for which Murphy is relied upon would have been recognized in Inoue by one of ordinary skill in the art at the time the invention was made.

As discussed above, the semiconductor device in Inoue comprises source/drain regions 29 and 30, which are formed prior to the deposition of

cobalt film 32 (Inoue - fig. 6B and col. 9, lines 40-47 and 56-59). Diffusion of dopant impurities in the source/drain regions occurs during subsequent high temperature processes. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Inoue and Agnello in view of Murphy by depositing the cobalt film at low temperatures, as taught by Murphy, because the low temperature deposition process helps to reduce diffusion of dopant impurities in the source/drain regions.

Claim 19 is unpatentable over the combination of Inoue, Agnello, and Murphy as applied to claims 13-15 above.

Response to Arguments

7. Applicant's arguments filed 27 April 2005 have been fully considered but they are not persuasive. Applicant argues that the Inoue reference does not teach forming the cobalt on a bare silicon surface. However, Inoue discloses a step of removing a native oxide prior to forming the cobalt surface (col. 10, lines 48-51).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the

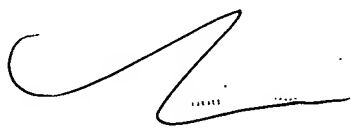
advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
11 July 2005



Mary Wilczewski
Primary Examiner